REMARKS

This paper is responsive to the Non-Final Office Action dated November 10, 2004. Claims 1-42 were examined. Claims 5-7 and 28-31 stand rejected under 35 U.S.C. § 112, second paragraph. Claims 1, 41, and 42 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,288,950 to Koike. Claims 2-7 are objected to as being dependent upon a rejected base claim. Claims 8-27 and 33-40 are allowed. Claims 28-31 would be allowable if rewritten to overcome the rejections under 35 U.S.C. § 112, second paragraph.

Amendments to the Specification

The specification is amended to correct typographical errors. No new matter is added.

Amendments to the Drawings

Figure 2 has been amended to indicate SA_L, consistent with the specification. No new matter is added.

Rejections Under 35 U.S.C. § 112, second paragraph

Claims 5-7 and 28-31 stand rejected under 35 U.S.C. § 112, second paragraph. These claims are amended to provide antecedent basis. Accordingly, Applicants respectfully request that the rejection of these claims be withdrawn.

Rejections Under 35 U.S.C. § 102(b)

Claims 1, 41, and 42 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,288,950 to Koike. Regarding claim 1, Applicants respectfully maintain that Koike, alone or in combination with other reference of record, fails to teach or suggest

> a test block configured to characterize in situ a sensing offset of a sensing circuit including a cross-coupled pair of transistors,

as recited by claim 1. The Office Action relies on FIG. 6 of Koike to supply this teaching. This portion of Koike teaches an FeRAM device including sense amplifier 92, offset circuit 61, and

offset control circuit 62. The offset circuit of Koike applies an offset voltage independent of voltages at the bit lines to a pair of bit lines to reduce the difference in potential between the pair of bit lines before the sense amplifiers are operated. (Abstract; col. 5, line 28-col. 6 line 24) After an offset voltage is applied to the bit lines of Koike, a high-reliability test is performed. Nowhere does Koike teach or suggest characterizing in situ a sensing offset of a sensing circuit including a cross-coupled pair of transistors, as required by claim 1. Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon be withdrawn.

Regarding claim 41, Applicants respectfully maintain that Koike, alone or in combination with other reference of record, fails to teach or suggest

> means for characterizing a magnitude of a sensing offset in a sensing circuit that includes a cross-coupled pair of transistors,

as required by claim 41. The Office Action relies on FIG. 6 of Koike to supply this teaching. This portion of Koike teaches an FeRAM device including sense amplifier 92, offset circuit 61, and offset control circuit 62. The offset circuit of Koike applies an offset voltage independent of voltages at the bit lines to a pair of bit lines to reduce the difference in potential between the pair of bit lines before the sense amplifiers are operated. (Abstract; col. 5, line 28-col. 6 line 24) After an offset voltage is applied to the bit lines of Koike, a high-reliability test is performed. Nowhere does Koike teach or suggest characterizing a magnitude of a sensing offset in a sensing circuit including a cross-coupled pair of transistors, as required by claim 41. Accordingly, Applicants respectfully request that the rejection of claim 41 and all claims dependent thereon be withdrawn.

Allowable Subject Matter

Applicants appreciate the indication of allowable subject matter in claims 2-7 and 28-31. Applicants believe claims 2-7 depend from an allowable base claim and are allowable for at least this reason.

Claims 28-31 are amended to overcome the rejections under 35 U.S.C. § 112, second paragraph.

Applicants appreciate the allowance of claims 8-27 and 33-40.

In summary, claims 1-42 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

☒ deposited with the US Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Nicole Teitler Cave 1/4/05
Nicole Teitler Cave Date

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Respectfully submitted,

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AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings include changes to Fig(s). 2 and replace the original sheet(s) including such figures.

Attachment(s): Replacement Sheet including amended Fig. 2; and
Annotated Sheet showing changes to Fig. 2.

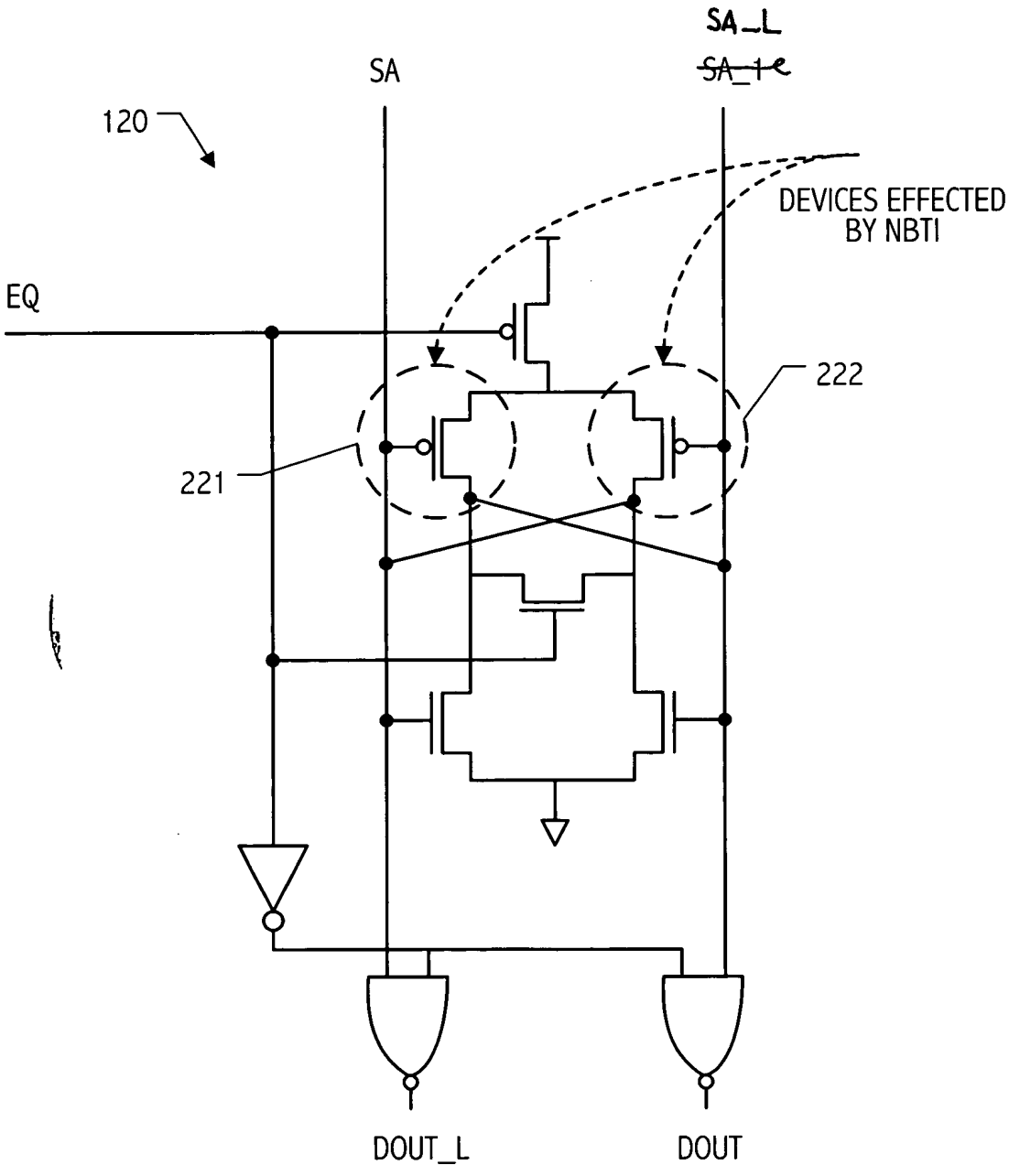

FIG. 2